

Fig. 1C
PRIOR ART

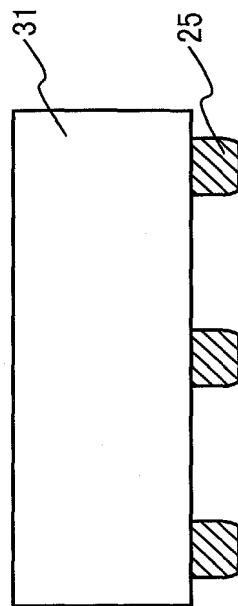


Fig. 1D
PRIOR ART

Fig. 2C

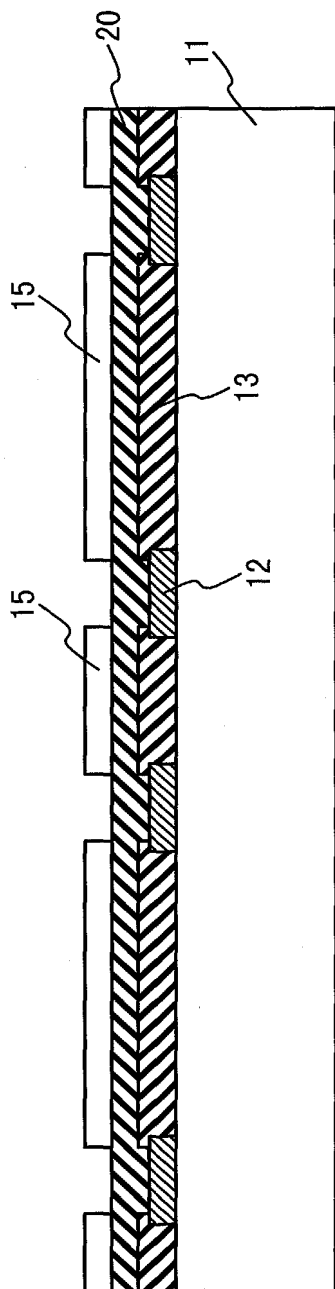


Fig. 2D

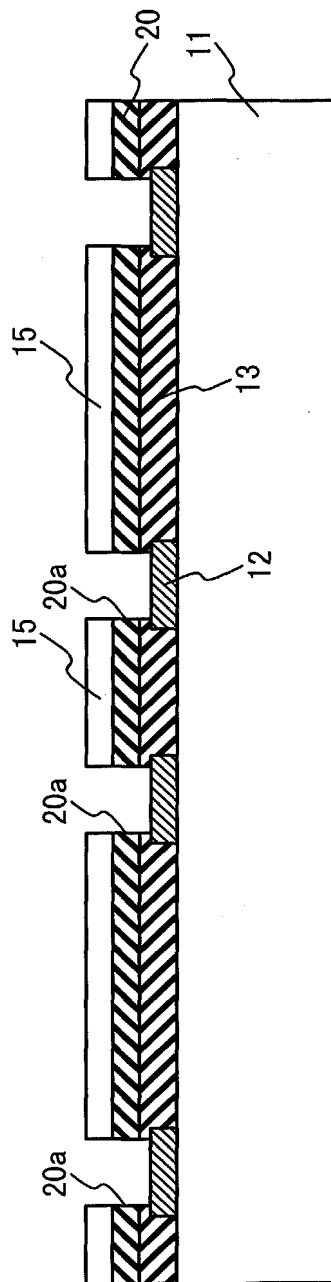


Fig. 2G

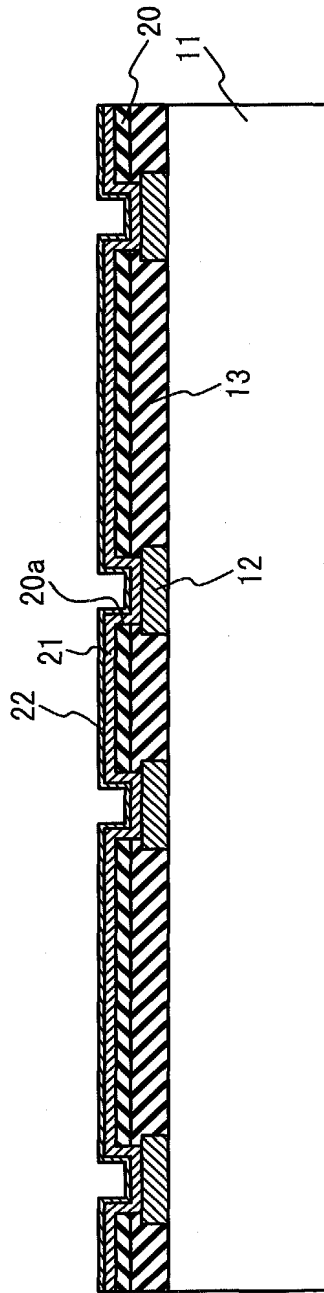
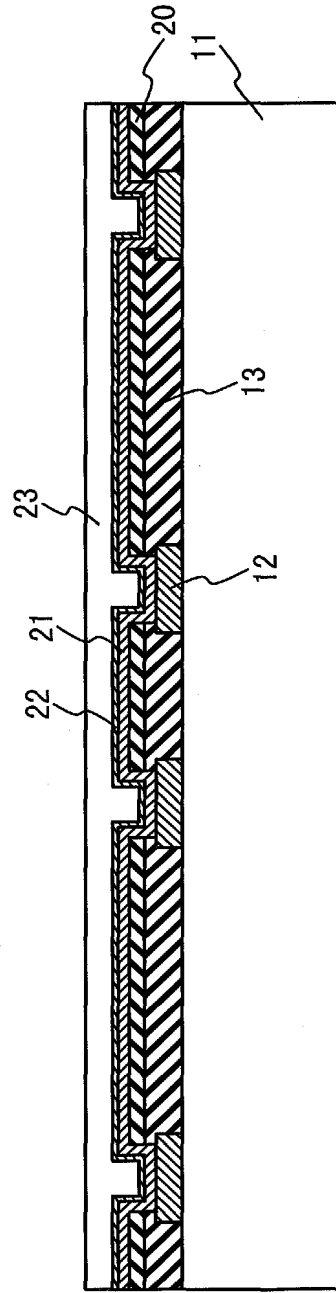


Fig. 2H



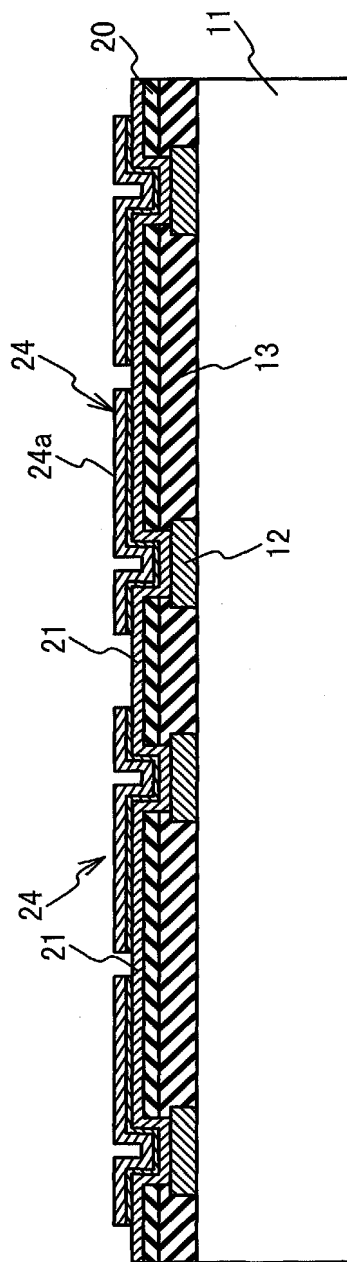


Fig. 2M

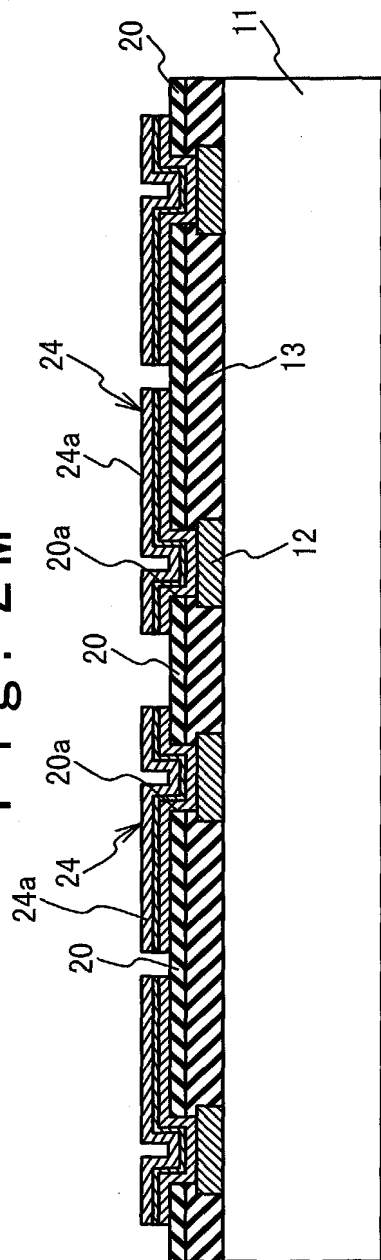
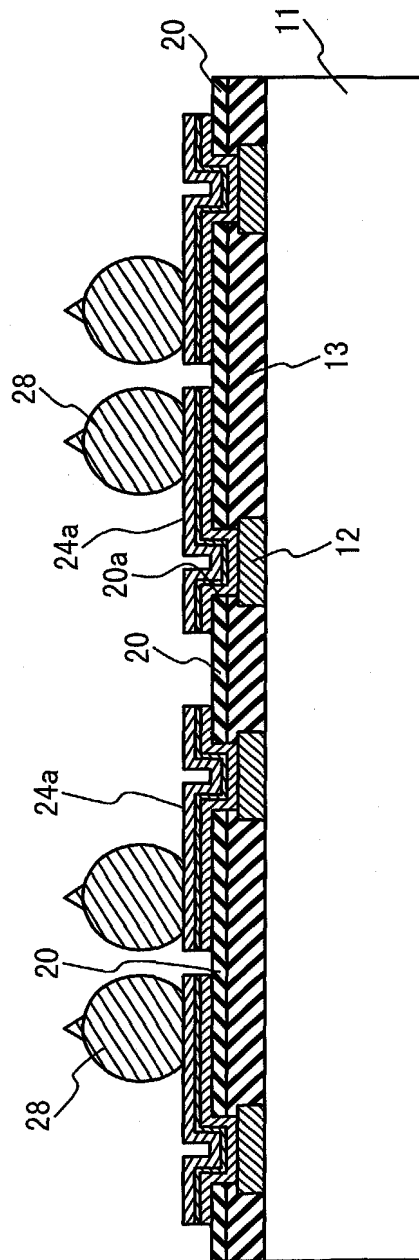


Fig. 2N



Fi. 20

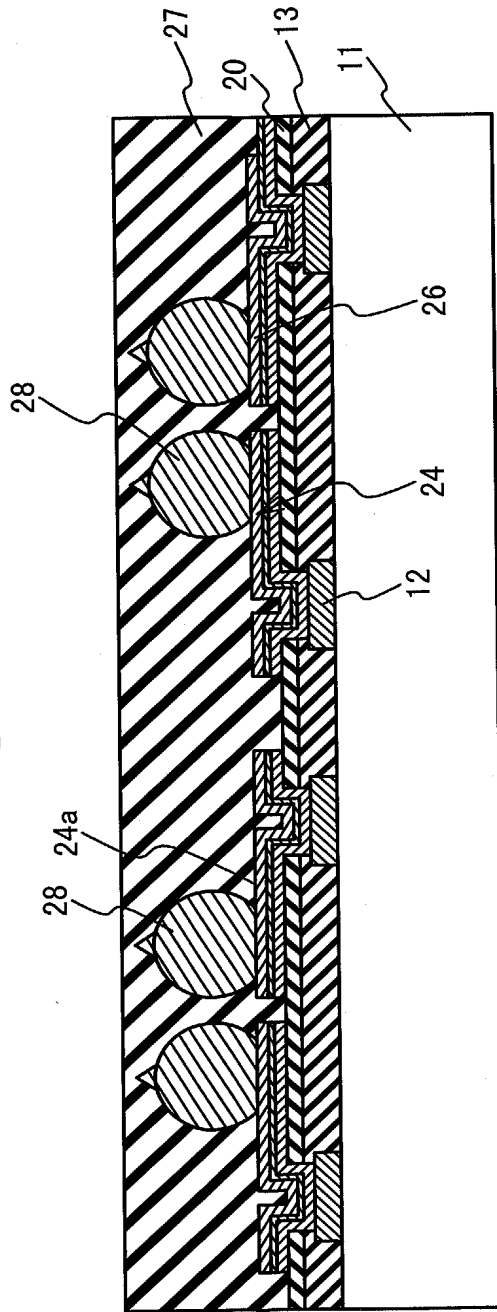
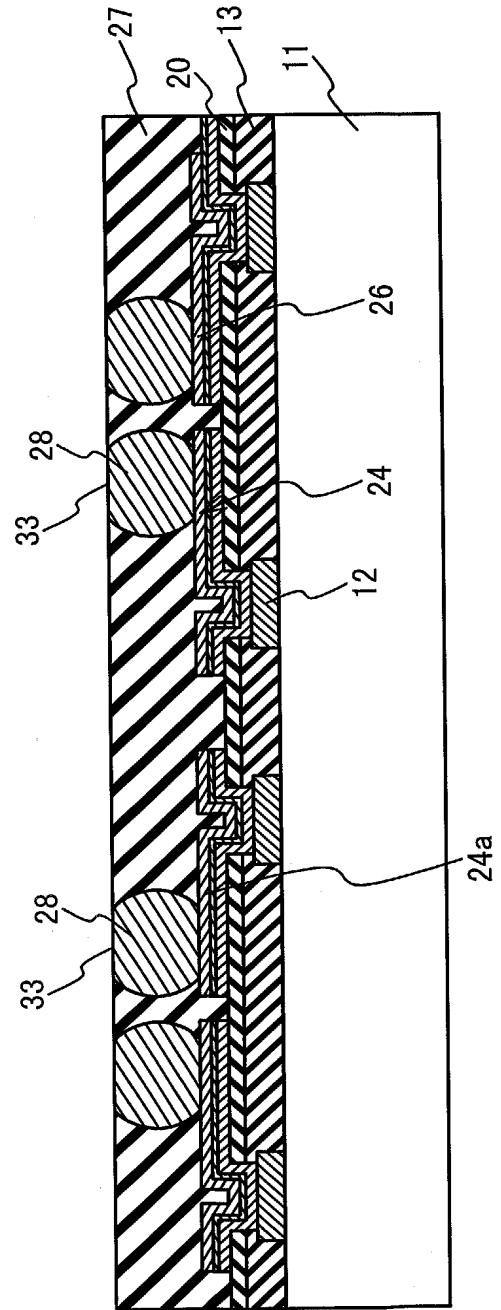
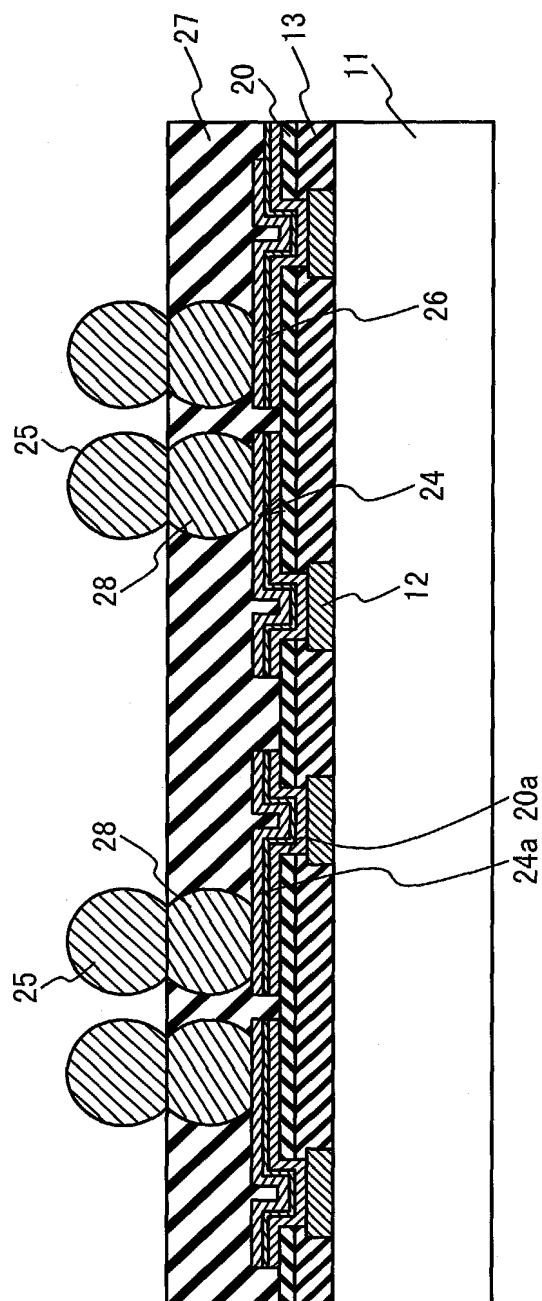


Fig. 2P





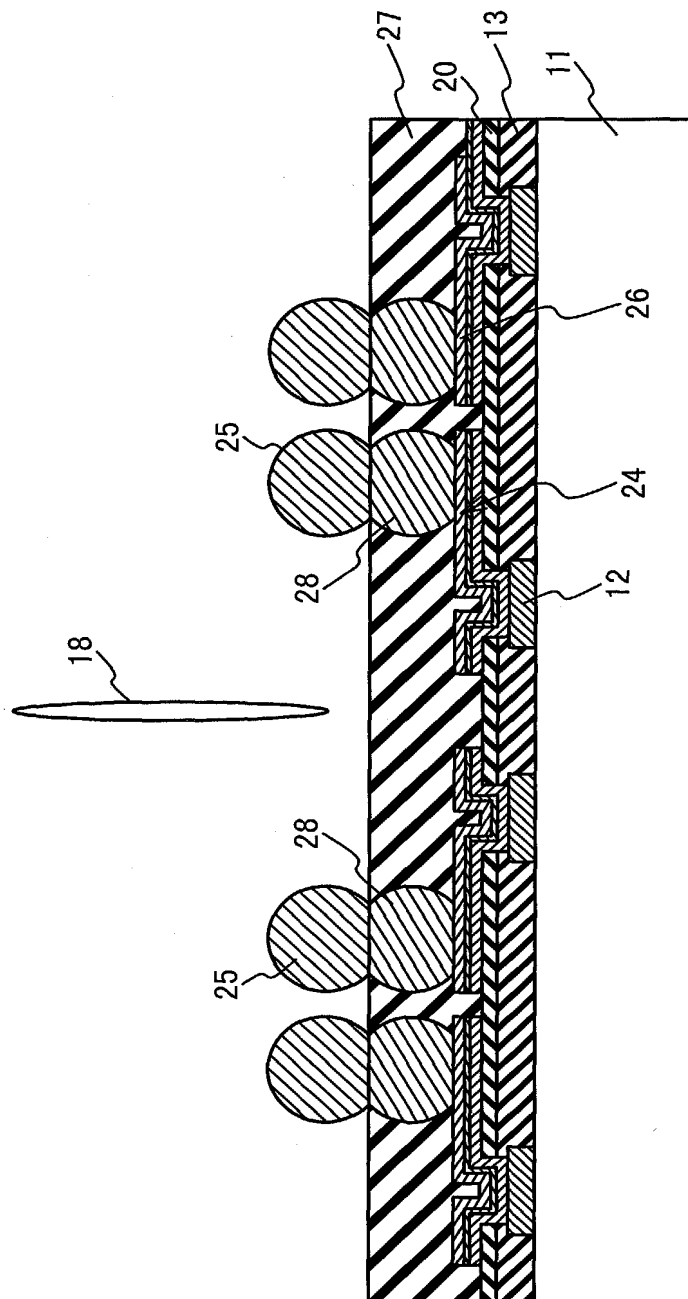
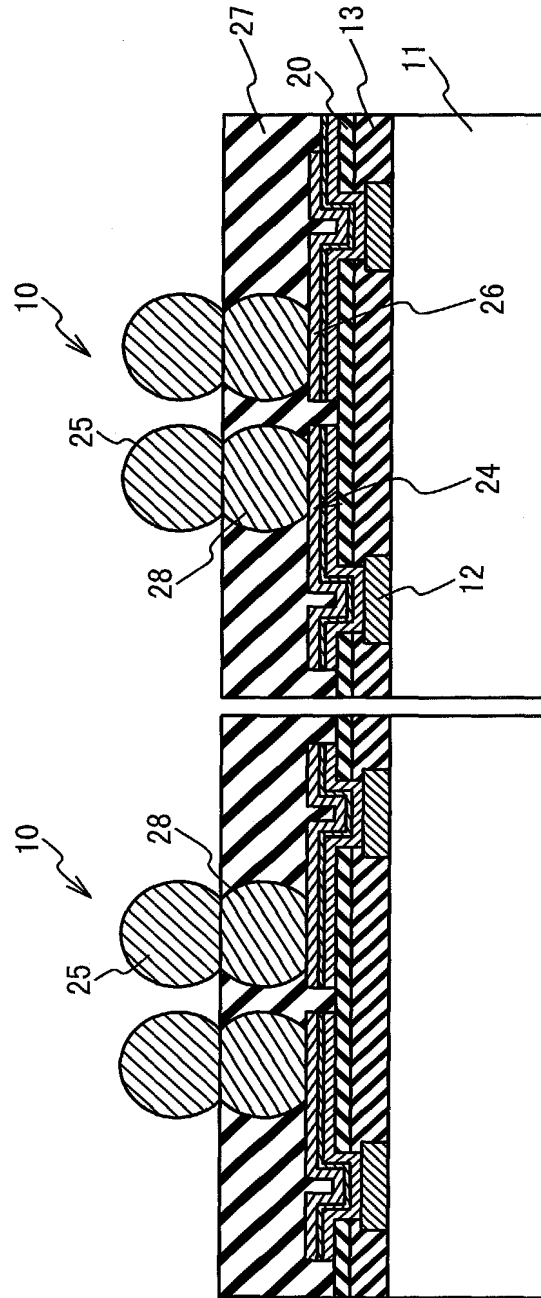


Fig. 2S



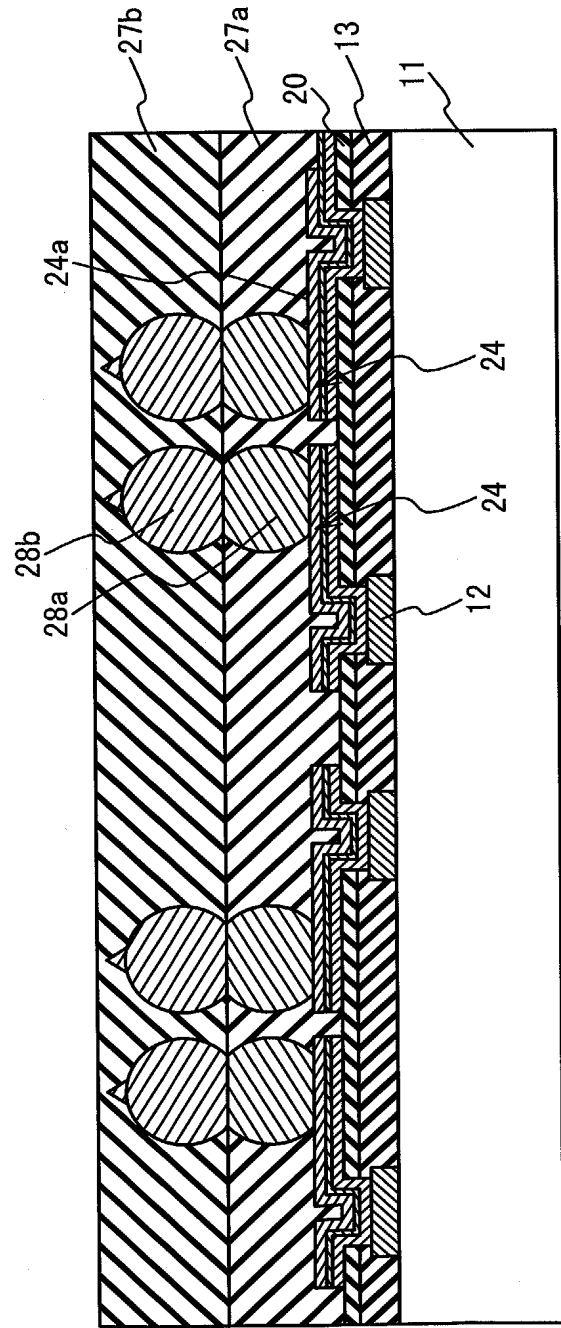


Fig. 3E

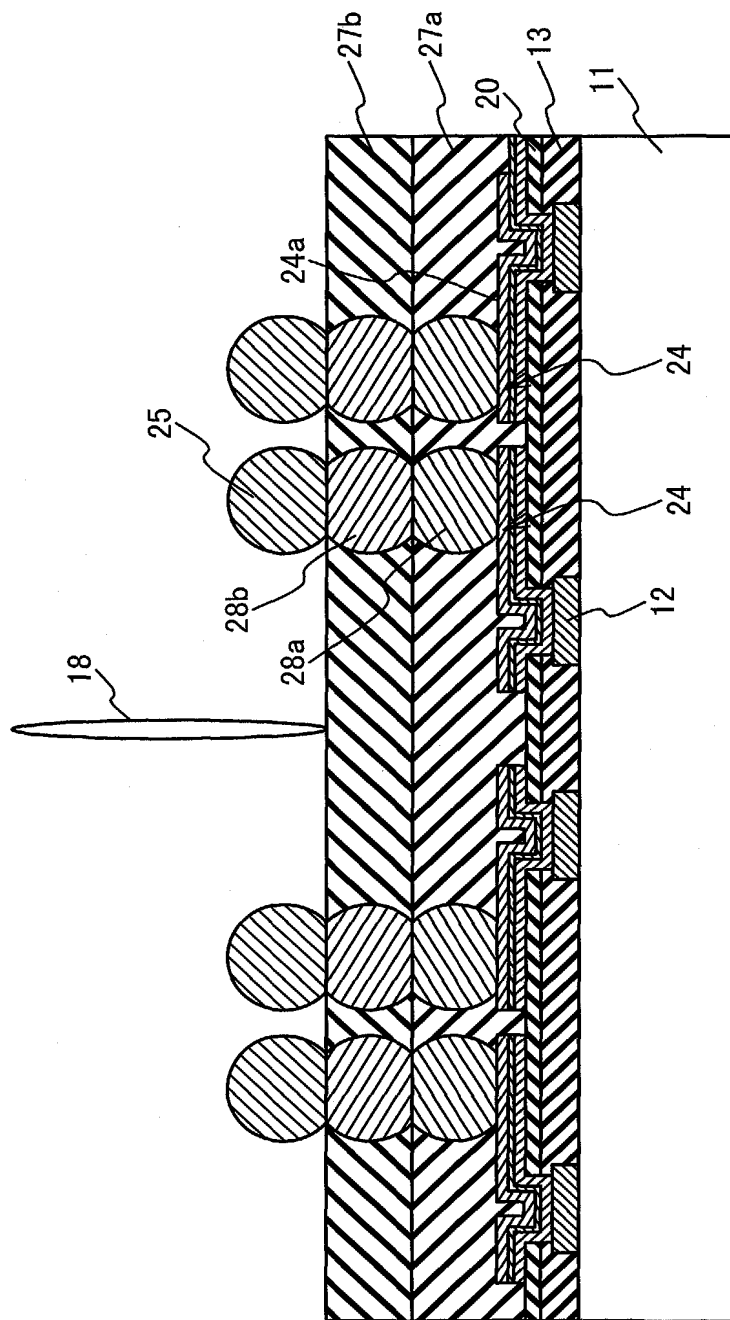


Fig. 3F

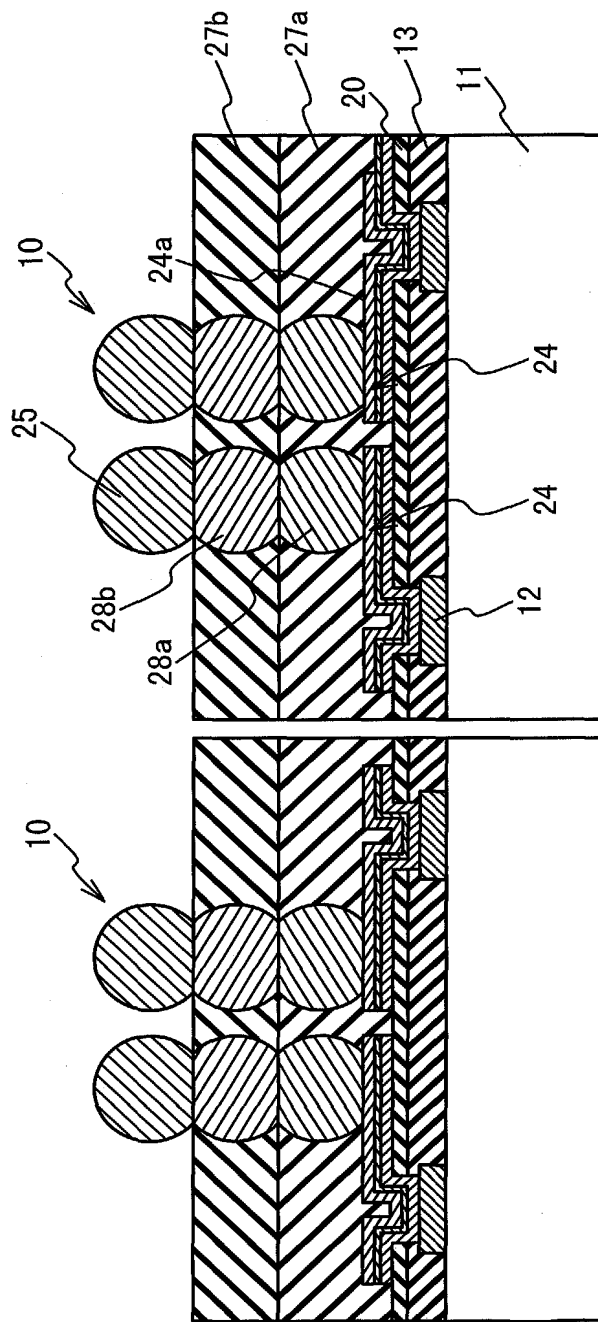


Fig. 4A

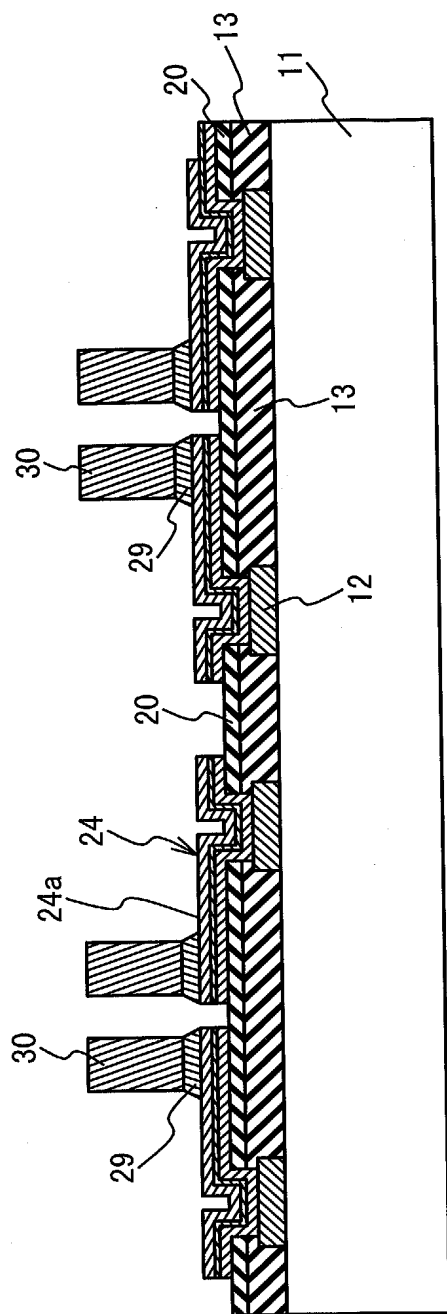


Fig. 4B

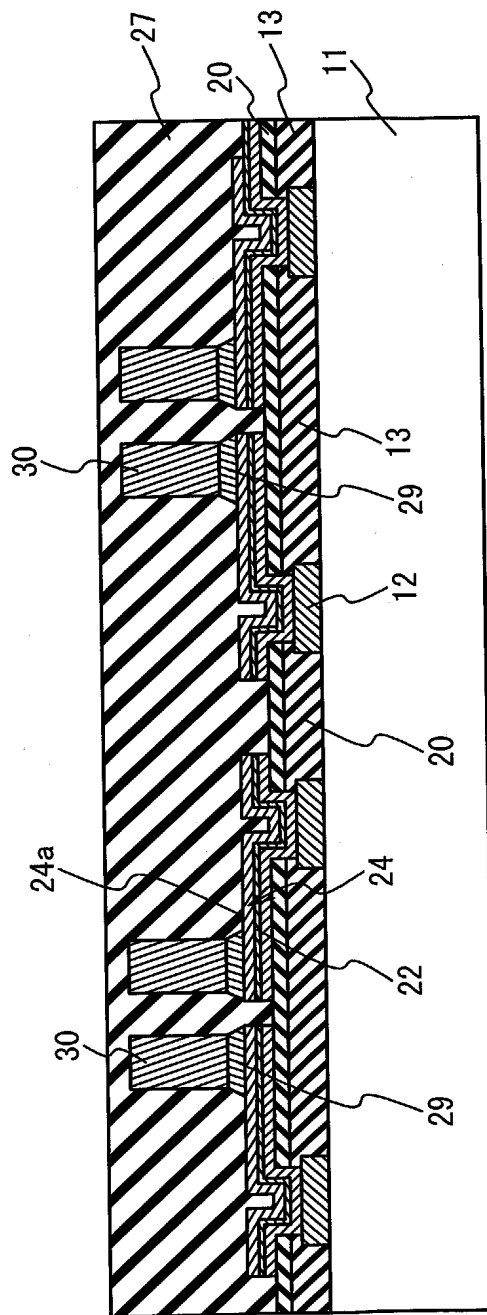


FIG. 4C is a cross-sectional view of a semiconductor device in a first state. The device includes a substrate 11, a gate stack 12, and a gate electrode 13. A channel region 20 is formed in the substrate 11 beneath the gate stack 12. A source region 22 and a drain region 24 are formed in the substrate 11 on either side of the channel region 20. A first conductive layer 25 is formed on the top surface of the source region 22 and the drain region 24. A second conductive layer 26 is formed on the top surface of the channel region 20. A third conductive layer 27 is formed on the top surface of the gate stack 12. A fourth conductive layer 28 is formed on the top surface of the gate stack 12. A fifth conductive layer 29 is formed on the top surface of the gate stack 12. A sixth conductive layer 30 is formed on the top surface of the gate stack 12. A seventh conductive layer 31 is formed on the top surface of the gate stack 12. An eighth conductive layer 32 is formed on the top surface of the gate stack 12. A ninth conductive layer 33 is formed on the top surface of the gate stack 12. A tenth conductive layer 34 is formed on the top surface of the gate stack 12.

Fig. 4C

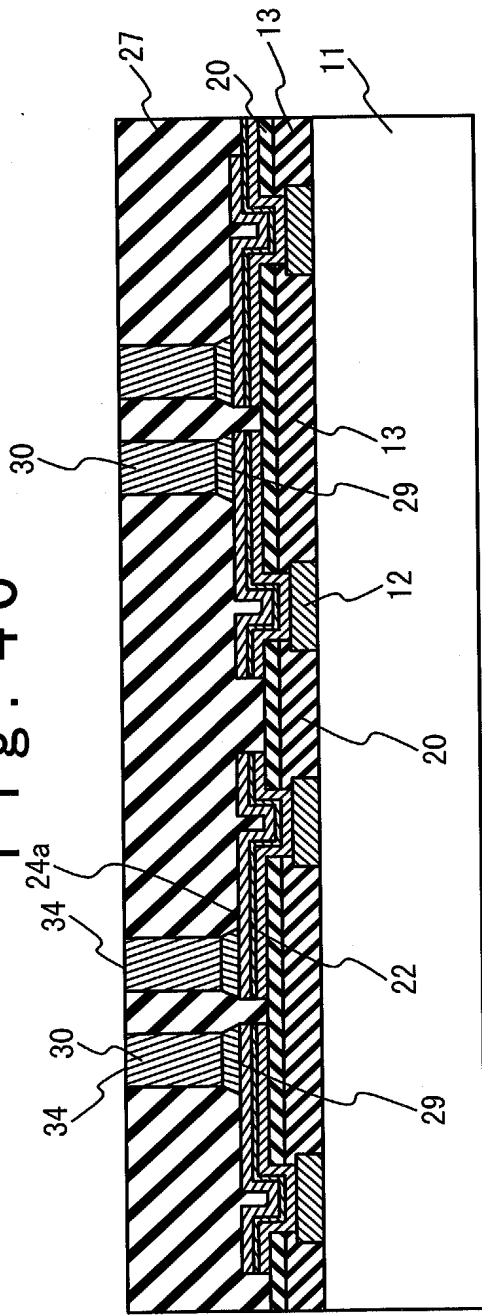


Fig. 4D

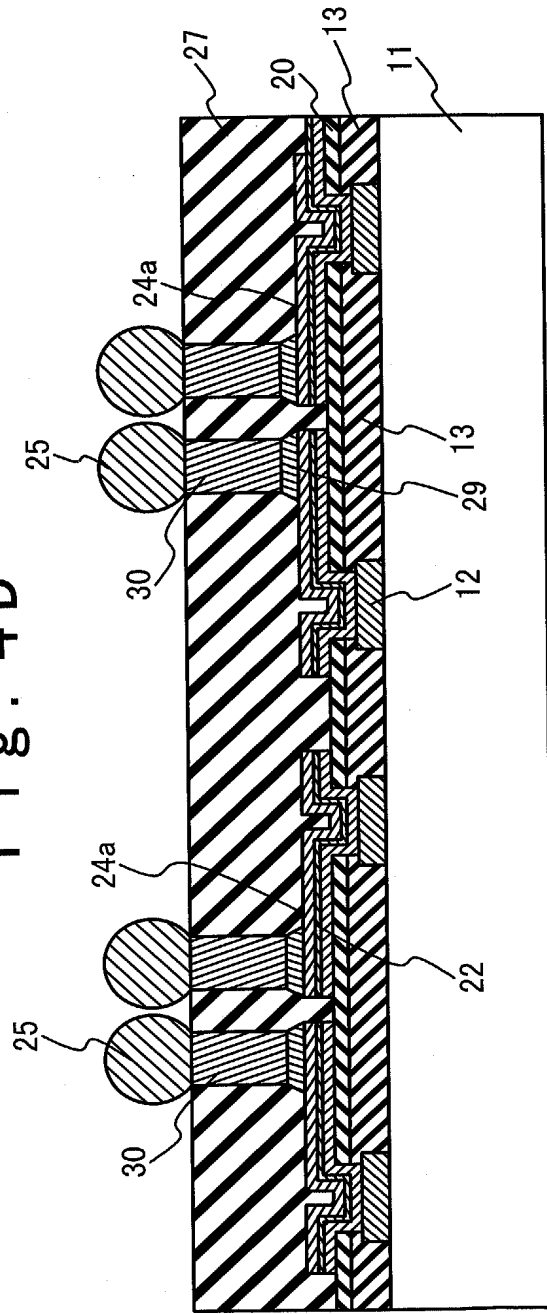


Fig. 4E

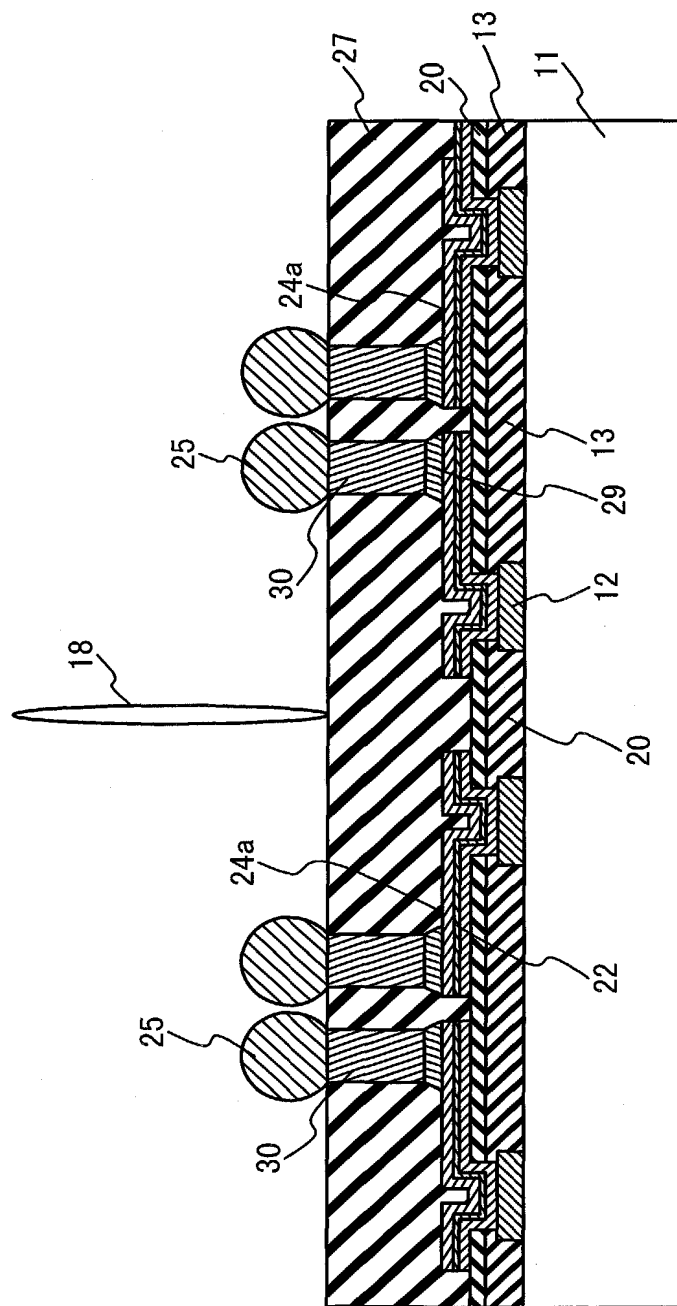


Fig. 4F

